What is claimed is:

1. An electronic device comprising:

a data receiver having a trip point adjustor; and

a data corrector coupled to the data receiver for adaptively providing trip point adjustment information to the trip point adjustor.

2. The electronic device of claim 1, further comprising a latch coupled between the data corrector and the data receiver for conditionally providing trip point adjustment information to the trip point adjustor of the data receiver.

3. The electronic device of claim 1, wherein the trip point adjustment information comprises analog control voltages.

4. An electronic device comprising:

a plurality of data receivers, each data receiver having a trip point adjustor; and

a data corrector coupled to each data receiver for adaptively providing trip point adjustment information to the trip point adjustor of each data receiver, the data corrector comprising:

a first ancillary data receiver having a first trip point adjustor;

a second ancillary data receiver having a second trip point adjustor;

a corrector controller coupled to the first trip point adjustor of the first ancillary data receiver and coupled to the second trip point adjustor of the second ancillary data receiver for adaptively providing trip point adjustment vectors.

5. The electronic device of claim 4, further comprising a latch coupled between the data corrector and each data receiver of the plurality of data receivers for conditionally providing trip point adjustment information to the trip point adjustor of each data receiver of the plurality of data receivers.

6. The electronic device of claim 5, wherein the trip point adjustment information comprises trip point adjustment vectors having been provided to the first and second ancillary data receivers without change for a number of adjustment cycles.

7. An integrated circuit comprising:

a data receiver having a trip point adjustor; and

a data corrector coupled to the data receiver for adaptively providing trip point adjustment signals to the trip point adjustor.

8. An integrated circuit comprising:

a first transistor pair having a first p-type MOS transistor coupled to a first n-type MOS transistor at a first node, a gate of the first p-type MOS transistor coupled to a gate of the first n-type MOS transistor;

a second transistor pair having a second p-type MOS transistor coupled to a second n-type MOS transistor at a second node, a gate of the second p-type MOS transistor coupled to a gate of the second n-type MOS transistor, the second p-type MOS transistor of the second transistor pair coupled to the first p-type MOS transistor of the first transistor pair at a third node, the second n-type MOS transistor of the second transistor pair coupled to the first n-type MOS transistor of the first transistor pair at a fourth node;

a third p-type MOS transistor coupled to the third node;

a third n-type MOS transistor coupled between the fourth node and ground having a gate coupled to a gate of the third p-type MOS transistor at the first node;

a plurality of series configured n-type MOS transistor pairs coupled between the first node and ground; and

a plurality of series configured p-type MOS transistor pairs coupled between a first voltage and the first node, wherein activating the plurality of series configured n-type MOS transistor pairs and the plurality of series configured p-type MOS transistor pairs adjusts a voltage at the first node.

9. The integrated circuit of claim 8, further comprising;

a voltage reference port coupled to the gate of the first p-type MOS transistor of the first transistor pair capable of providing a voltage reference signal; and

a data port coupled to the gate of the second p-type MOS transistor of the second transistor pair capable of providing a data signal.

10. A memory device comprising:

a data receiver having a trip point adjustor; and

a data corrector coupled to the data receiver for adaptively providing trip point adjustment information to the trip point adjustor of the data receiver.

11. The memory device of claim 10, further comprising a latch coupled between the data corrector and the data receiver for conditionally providing trip point adjustment information to the trip point adjustor of the data receiver.

12. A memory device comprising:

a plurality of data receivers, each data receiver having a trip point adjustor; and

a data corrector coupled to each data receiver for adaptively providing trip point adjustment information to the trip point adjustor of each data receiver, the data corrector comprising:

a first ancillary data receiver having a first trip point adjustor;

a second ancillary data receiver having a second trip point adjustor;

a phase detector coupled to an output of the first ancillary data receiver and coupled to an output of the second ancillary data receiver, wherein the phase detector compares an output signal of the first ancillary data receiver with an output signal from the second ancillary data receiver; and

a corrector controller coupled to the phase detector for receiving comparison information, the corrector controller coupled to the first trip point adjustor of the first ancillary data receiver and coupled to the second trip point adjustor of the second ancillary data receiver for adaptively providing trip point adjustment vectors.

13. A data receiver comprising:

a receiver having a trip point; and

a trip point adjustor coupled to the receiver for adaptively adjusting the trip point of the receiver.

14. The data receiver of claim 13, wherein the receiver comprises:

a first transistor pair having a first p-type MOS transistor coupled to a first n-type MOS transistor at a first node, a gate of the first p-type MOS transistor coupled to a gate of the first n-type MOS transistor;

a second transistor pair having a second p-type MOS transistor coupled to a second n-type MOS transistor at a second node, a gate of the second p-type MOS transistor coupled to a gate of the second n-type MOS transistor, the second p-type MOS transistor of the second transistor pair coupled to the first p-type MOS transistor of the first transistor pair at a third node, the second n-type MOS transistor of the second transistor pair coupled to the first n-type MOS transistor of the first transistor pair at a fourth node;

a third p-type MOS transistor coupled to the third node; and

a third n-type MOS transistor coupled between the fourth node and ground having a gate coupled to a gate of the third p-type MOS transistor at the first node.

15. The data receiver of claim 13, wherein the receiver comprises a differential pair receiver.

16. The data receiver of claim 13, wherein the receiver comprises:

a differential amplifier;

a voltage reference port coupled to an input of the differential amplifier; and

a data port coupled to another input of the differential amplifier.

17. The data receiver of claim 16, wherein the trip point adjustor comprises:

a plurality of series configured n-type MOS transistor pairs coupled to a node of the differential amplifier; and

a plurality of series configured p-type MOS transistor pairs coupled to the differential amplifier at the node, wherein activating the plurality of n-type MOS transistor pairs and the plurality of p-type MOS transistor pairs adjusts a voltage at the node.

18. The data receiver of claim 17, wherein the trip point adjustor further includes a plurality of adjustment ports configured in two sets, one set coupled to the plurality of series configured n-type MOS transistor pairs in a one to one manner, the other set coupled to the plurality of series configured p-type MOS transistor pairs in a one to one manner, wherein the plurality of series configured n-type MOS transistor pairs equals the plurality of series configured p-type MOS transistor pairs, the two sets of adjustment ports capable of providing signals to activate the plurality of n-type MOS transistor pairs and the plurality of p-type MOS transistor pairs.

19. The data receiver of claim 17, wherein the plurality of series configured n-type MOS transistor pairs is four, and the plurality of series configured p-type MOS transistor pairs is four.

20. The data receiver of claim 17, wherein the voltage at the node is adjusted in a range from about minus 200 mV to about positive 200 mV.

21. The data receiver of claim 17, wherein the plurality of series configured n-type MOS transistor pairs comprise a weighted set of series configured n-type MOS transistor pairs, and the plurality of series configured p-type MOS transistor pairs comprise a weighted set of series configured p-type MOS transistor pairs.

22. The data receiver of claim 21, wherein the weighted set of series configured n-type MOS transistor pairs and the weighted set of series configured p-type MOS transistor pairs are weighted based on a width to a length ratio for each n-type MOS transistor acting as a load transistor in the series configured n-type MOS transistor pairs and for each p-type MOS transistor acting as a load transistor in the series configured p-type MOS transistor pairs.

23. A data receiver comprising:

a first transistor pair having a first p-type MOS transistor coupled to a first n-type MOS transistor at a first node, a gate of the first p-type MOS transistor coupled to a gate of the first n-type MOS transistor;

a second transistor pair having a second p-type MOS transistor coupled to a second n-type MOS transistor at a second node, a gate of the second p-type MOS transistor coupled to a gate of the second n-type MOS transistor, the second p-type MOS transistor of the second transistor pair coupled to the first p-type MOS transistor of the first transistor pair at a third node, the second n-type MOS transistor of the second transistor pair coupled to the first n-type MOS transistor of the first transistor pair at a fourth node;

a third p-type MOS transistor coupled to the third node;

a third n-type MOS transistor coupled between the fourth node and ground having a gate coupled to a gate of the third p-type MOS transistor at the first node;

a plurality of series configured n-type MOS transistor pairs coupled between the first node and ground; and

a plurality of series configured p-type MOS transistor pairs coupled between a first voltage and the first node, wherein activating the plurality of series configured n-type MOS transistor pairs and the plurality of series configured p-type MOS transistor pairs adjusts a voltage at the first node.

24. The data receiver of claim 23, wherein the plurality of series configured n-type MOS transistor pairs comprise a weighted set of series configured n-type MOS

transistor pairs, and the plurality of series configured p-type MOS transistor pairs comprise a weighted set of series configured p-type MOS transistor pairs.

25. The data receiver of claim 24, wherein the weighted set of series configured n-type MOS transistor pairs and the weighted set of series configured p-type MOS transistor pairs are weighted based on a width to a length ratio for each n-type MOS transistor acting as a load transistor in the series configured n-type MOS transistor pairs and for each p-type MOS transistor acting as a load transistor in the series configured p-type MOS transistor pairs.

26. A trip point adjustor comprising:

a plurality of series configured n-type MOS transistor pairs coupled between a node and ground; and

a plurality of series configured p-type MOS transistor pairs coupled between a first voltage and the node, wherein activating the plurality of series configured n-type MOS transistor pairs and the plurality of series configured p-type MOS transistor pairs adjusts a voltage at the node.

27. The trip point adjustor of claim 26, wherein the plurality of series configured – type MOS transistor pairs is four, and the plurality of series configured p-type MOS transistor pairs is four.

28. The trip point adjustor of claim 26, wherein the plurality of series configured – type MOS transistor pairs comprise a weighted set of series configured n-type MOS transistor pairs, and the plurality of series configured p-type MOS transistor pairs comprise a weighted set of series configured p-type MOS transistor pairs.

29. The trip point adjustor of claim 28, wherein the weighted set of series configured n-type MOS transistor pairs and the weighted set of series configured p-type MOS transistor pairs are weighted based on a width to a length ratio for each n-type

MOS transistor acting as a load transistor in the series configured n-type MOS transistor pairs and for each p-type MOS transistor acting as a load transistor in the series configured p-type MOS transistor pairs.

30. A data corrector comprising:

a first ancillary data receiver;

a second ancillary data receiver; and

a corrector controller coupled to the first ancillary data receiver and coupled to the second ancillary data receiver for adaptively providing adjustment vectors to the first ancillary data receiver and to the second ancillary data receiver.

31. The data corrector of claim 30, wherein the corrector controller includes control logic for sending the adjustment vectors to data receivers external to the data corrector after determining that the adjustment vectors have been provided to the first and second ancillary data receivers without change for a number of adjustment cycles.

32. The data corrector of claim 30, wherein the adjustment vectors to the first ancillary data receiver and to the second ancillary data receiver provide signals to adjust trip points of the first ancillary data receiver and the second ancillary data receiver.

33. The data corrector of claim 30, wherein the first ancillary data receiver includes a data port configured for receiving a first clock signal, the second ancillary data receiver includes a data port configured for receiving a second clock signal, the first ancillary data receiver coupled to the second ancillary data receiver at a voltage reference port capable of receiving a reference voltage.

34. The data corrector of claim 30, wherein the data corrector further includes a phase detector coupled to an output of the first ancillary data receiver and coupled to an output of the second ancillary data receiver, wherein the phase detector compares an output signal of the first ancillary data receiver with an output signal from the second

ancillary data receiver.

35. The data corrector of claim 34, wherein the data corrector further includes a filter coupled between the phase detector and the corrector controller, wherein the filter controls sending an output signal from the phase detector to the corrector controller based on a predetermined setting.

36. The data corrector of claim 35, wherein the filter includes a counter for determining whether the output of the phase detector has maintained a constant level for a plurality of clock pulses.

37. The data corrector of claim 36, wherein the plurality of clock pulses is four.

38. A data corrector comprising:

a first ancillary data receiver having a first trip point adjustor;

a second ancillary data receiver having a second trip point adjustor;

a phase detector coupled to an output of the first ancillary data receiver and coupled to an output of the second ancillary data receiver, wherein the phase detector compares an output signal of the first ancillary data receiver with an output signal from the second ancillary data receiver; and

a corrector controller coupled to the phase detector for receiving comparison information, the corrector controller coupled to the first and second trip point adjustors for adaptively providing trip point adjustment vectors to the first trip point adjustor and to the second trip point adjustor.

39. The data corrector of claim 38, wherein the first ancillary data receiver includes a data port configured for receiving a first clock signal, the second ancillary data receiver includes a data port configured for receiving a second clock signal, the first ancillary data receiver coupled to the second ancillary data receiver at a voltage reference port capable of receiving a reference voltage.

40. The data corrector of claim 38, wherein the data corrector further includes a filter coupled between the phase detector and the corrector controller, wherein the filter controls sending an output signal from the phase detector to the data corrector based on a predetermined setting.

41. The data corrector of claim 38, wherein the corrector controller includes control logic for sending the adjustment vectors to data receivers external to the data corrector after determining that the adjustment vectors have been provided to the first and second trip point adjustors without change for a number of adjustment cycles.

42. A phase detector comprising:

a means for balancing two signals; and

a means for comparing a zero crossing of the two signals, the means for balancing two signals coupled to the means for comparing a zero crossing of the two signals.

43. The phase detector of claim 42, wherein comparing a zero crossing of the two signals comprises determining when a transition of a rising edge on one signal is concurrent with a transition of a falling edge of the other signal.

44. The phase detector of claim 42, wherein the means for balancing two signals comprises:

a first NAND gate having an output;

a second NAND gate having an output;

a first n-type capacitor coupled between ground and the output of the first NAND gate;

a second n-type capacitor coupled between ground and the output of the second NAND gate;

a first inverter coupled to the output of the first NAND gate;

a second inverter coupled to the output of the second NAND gate;

a third n-type capacitor coupled between ground and an output of the first inverter;

a fourth n-type capacitor coupled between ground and an output of the second inverter; and

a p-type capacitor coupled between a voltage and the output of the first inverter, wherein the n-type and p-type capacitors have capacitances set such that, for a first clock signal at an input to the first NAND gate and a second clock signal at an input to the second NAND gate, a rise time and a fall time for the first clock at an output of the first inverter is approximately equal to a rise time and a fall time for the second clock at an output of the second inverter.

45. The phase detector of claim 42, wherein the means for comparing a zero crossing of the two signals comprises:

a NAND gate having an output coupled to a first inverter; and

a NOR gate having an output coupled to a second inverter, the second inverter having an output coupled to an input of the NAND gate, an input of the NOR gate coupled to an output of the first inverter.

46. The phase detector of claim 45, wherein the means for comparing a zero crossing of the two signals further comprises:

a third inverter coupled to the output of the NAND gate;

a fourth inverter coupled in series to the output of the third inverter;

a fifth inverter coupled to the output of the NOR gate;

a first p-type MOS transistor coupled in series with the output of the fourth inverter;

a first n-type MOS transistor coupled between the first p-type MOS transistor and a node, a gate of the first p-type MOS transistor coupled to a gate of the first n-type MOS transistor, the gate of the first p-type MOS transistor coupled to an output of the fifth inverter;

a second p-type MOS transistor coupled in series with the output of the fifth

inverter; and

a second n-type MOS transistor coupled between the second p-type MOS transistor and the node, a gate of the second p-type MOS transistor coupled to a gate of the second n-type MOS transistor, the gate of the second p-type MOS transistor coupled to an output of the fourth inverter.

47. A balancing circuit for balancing two signals comprising:

a first NAND gate having an output;

a second NAND gate having an output;

a first n-type capacitor coupled between ground and the output of the first NAND gate;

a second n-type capacitor coupled between ground and the output of the second NAND gate;

a first inverter coupled to the output of the first NAND gate;

a second inverter coupled to the output of the second NAND gate;

a third n-type capacitor coupled between ground and an output of the first inverter;

a fourth n-type capacitor coupled between ground and an output of the second inverter; and

a p-type capacitor coupled between a voltage and the output of the first inverter, wherein the n-type and p-type capacitors have capacitances set such that, for a first clock signal at an input to the first NAND gate and a second clock signal at an input to the second NAND gate, a rise time and a fall time for the first clock at an output of the first inverter is approximately equal to a rise time and a fall time for the second clock at an output of the second inverter.

48. A phase detection circuit for comparing a zero crossing of two signals comprising:

a NAND gate having an output coupled to a first inverter; and

a NOR gate having an output coupled to a second inverter, the second inverter

having an output coupled to an input of the NAND gate, an input of the NOR gate coupled to an output of the first inverter.

49. A processing system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

a plurality of data receivers, each data receiver having a trip point adjustor; and

a data corrector coupled to each data receiver for adaptively providing trip point adjustment information to the trip point adjustor of each data receiver.

50. A method of operating a data receiver having a data offset adjustment comprising:

providing a data signal to the data receiver;

providing clock signals to a data corrector;

generating adjustment information in the data corrector related to the received clock signals; and

conditionally sending the adjustment information to the data receiver.

51. The method of claim 50, wherein the clock signals are differential clock signals.

52. The method of claim 50, further comprising providing a reference voltage to the data receiver and the data corrector to provide a reference level for generating a first trip point in the data receiver and a plurality of trips points in the data corrector.

53. The method of claim 50, wherein the clock signals and the data signal originate from a common source.

54. The method of claim 53, wherein the common source comprises a common chipset.

55. A method of operating a data corrector comprising:

providing a first clock signal to a data port of a first ancillary data receiver, the first ancillary data receiver providing an output signal related to the first clock signal;

providing a second clock signal to a data port of a second ancillary data receiver, the second ancillary data receiver providing an output signal related to the second clock signal;

determining a difference between the output signals of the first and second ancillary data receivers; and

generating adjustment vectors correlated to the difference between the output signals of the first and second ancillary data receivers.

56. The method of claim 55, further comprising:

providing differential clock signals as the first clock signal and the second clock signal; and

providing a voltage reference to the first ancillary data receiver and to the second ancillary data receiver to set a reference level for a first trip point in the first ancillary data receiver and a second trip point in the second ancillary data receiver.

57. The method of claim 55, wherein determining a difference between the output signals of the first and second ancillary data receivers comprises detecting a zero crossing of the output signals of the ancillary data receivers.

58. The method of claim 55, further comprising providing the adjustment vectors to the first ancillary data receiver and to the second ancillary data receiver.

59. The method of claim 58, further comprising conditionally making available the adjustment vectors to data receivers external to the data corrector.

60. The method of claim 59, wherein conditionally making available the adjustment vectors to data receivers external to the data corrector comprises:

determining that the adjustment vectors provided to the first ancillary data receiver and to the second ancillary data receiver have remained constant for a predetermined number of adjustment cycles; and

making available the adjustment vectors to each data receiver external to the data corrector.

61. A method for operating a memory device having data receivers with data offset adjustment comprising:

providing a data signal to a data receiver;

providing a first clock signal to a data port of a first ancillary data receiver, the first ancillary data receiver having a first trip point, the first ancillary data receiver providing an output signal related to the first clock signal;

providing a second clock signal to a data port of a second ancillary data receiver, the second ancillary data receiver having a second trip point, the second ancillary data receiver providing an output signal related to the second clock signal;

determining a difference between the output signals of the first and second ancillary data receivers;

generating adjustment vectors correlated to the difference between the output signals of the first and second ancillary data receivers;

providing the adjustment vectors to the first and second ancillary data receivers to adjust the trip points of the first and second ancillary data receivers; and

conditionally sending the adjustment vectors to the data receiver.

62. The method of claim 61, further comprising:

providing differential clock signals as the first clock signal and the second clock signal; and

providing a voltage reference to the first ancillary data receiver and to the second ancillary data receiver to set a reference level for the first trip point in the first ancillary data receiver and a second trip point in the second ancillary data receiver.

63. The method of claim 61, wherein conditionally sending the adjustment vectors to the data receiver comprises:

determining that the adjustment vectors provided to the first ancillary data receiver and to the second ancillary data receiver have remained constant for a predetermined number of adjustment cycles;

determining if the data receiver is in a quiet period; and

providing the adjustment vector to the data receiver if the data receiver has been determined to be in a quiet period.

64. The method of claim 63, wherein the quiet period for a data receiver includes a time period during which the data receiver is not transferring data.